# SEMICONDUCTOR MEMORY DEVICE CAPABLE OF GENERATING VARIABLE CLOCK SIGNALS ACCORDING TO MODES OF OPERATION

## ABSTRACT OF DISCLOSURE

A semiconductor memory device comprising: an array of memory cells; an address input circuit for receiving an external address in response to an address clock signal; a selecting circuit for selecting a memory cell in response to an address output from the address input circuit; a data output circuit for outputting the data read out from the selected memory cell in response to first and second data clock signals; and an internal clock generating circuit for generating the address clock signal and the first and second data clock signals in response to an external clock signal and a complementary clock signal thereof, wherein the address clock signal and the first and second data clock signals have twice the frequency (or half the period) of the external clock signal when in a test mode.